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10/525,203	02/22/2005	Yuichi Takagi	SON-2815	7661
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/525,203

Applicant(s)

TAKAGI ET AL.

Examiner

DENNIS P. JOSEPH

Art Unit

2629

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 February 2009.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-28 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4, 7-14 and 17-28 is/are rejected.
- 7) ☒ Claim(s) 5, 6, 15 and 16 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SI-108)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

1. This Office Action is responsive to arguments for application No. 10/525,203 on February 23, 2009. Claims 1-28 are pending and have been examined.
2. A request for continued examination under 37 CFR 1.114 was filed in this application after appeal to the Board of Patent Appeals and Interferences, but prior to a decision on the appeal. Since this application is eligible for continued examination under 37 CFR 1.114 and the fee set forth in 37 CFR 1.17(e) has been timely paid, the appeal has been withdrawn pursuant to 37 CFR 1.114 and prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on February 23, 2009 has been entered.

Allowable Subject Matter

3. **Claims 5, 6, 15 and 16** objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections – 35 USC § 103

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 103(a) that forms the basis for the rejections under this section made in this Office action:
(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
 2. Ascertaining the differences between the prior art and the claims at issue.
 3. Resolving the level of ordinary skill in the pertinent art.
 4. Considering objective evidence present in the application indicating obviousness or nonobviousness.
5. **Claims 1-4, 7-14 and 17-28** rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi (6,332,661) in view of Hughes et al. (US 6,313,780 B1)

Yamaguchi teaches in Claim 1:

A current output type drive circuit for outputting a drive current to a driven object shared by being divided into a plurality of areas (**Figure 1 shows the current drivers used to drive the EL devices 51, 52, etc (read as a plurality of areas) ,**

comprising a plurality of drivers arranged corresponding to each the shared area of the driven object (**Figure 1, driver ICS 1, 2 and 3, Column 5, Lines 41-46) ,**

each driver comprising

an output means for outputting a supplied reference current and the drive current corresponding to image data to a corresponding shared area of the driven object (**Figure 1, output terminals 001-064, Column 5, Lines 41-46. The terminals output the current from the driver circuits to the pixel elements) , and**

a reference current source circuit (**Figure 1, reference current generation circuit 12. It is connected to each driver) ; but**

Yamaguchi does not explicitly teach the reference current source circuit is used “for sampling and holding the reference current input from a reference current input terminal, then supplying the same to the output means.”

However, sampling and holding circuitry and means is well known in the art, in conjunction with current mirrors, taught by Yamaguchi and disclosed in Figure 3, which shows circuitry within the reference current generation circuit 12. In addition, Yamaguchi teaches of the reference current input terminals IREF as shown in Figures 1 and 2.

To emphasize on this, in the same field of endeavor, current circuitry, Hughes teaches of using current memories M41 and M42 to sample and hold the input current sample, (Hughes, Column 2, Lines 35-48). During the four phases, the two memories sample and store (read as held) and then outputted accordingly. The reference terminals of Yamaguchi connect to the reference current generation circuit 12 and the sampling and holding means are processed within 12 and then output accordingly.

Therefore, it would be obvious to one of ordinary skill at the time of the invention to integrate the sampling and holding means by using the current memories, as taught by Hughes, with Yamaguchi's circuitry, with the motivation that is sampling and holding is a well known technique in the art. KSR teachings provide many principles here, such as known technique, simple substitution of parts, with regards to implementing the circuitry, suggestion in the prior art, Yamaguchi, etc. Applicant has also noted that this is well known as well. As for

implementing them with the current memories, Hughes notes that by using two memories, data will not be corrupted, so data loss can be prevented, (Hughes, Column 2, Lines 4-19)

Yamaguchi and Hughes teach in Claim 2:

A current output type drive circuit as set forth in claim 1, wherein said reference current source circuit (**Yamaguchi, Figure 1, reference current generation circuit 12**) comprises at least:

a current sampling circuit including a current memory for sampling and holding said reference current in accordance with a control signal (**Hughes, Figure 4 shows current memory M41**) and

a control circuit for outputting to said current sampling circuit a control signal for controlling write and read operations of said reference current of the current memory of said current sampling circuit. (**Hughes, Figure 4 shows the switches for each memory. It is obvious to one of skill that there is a control means for controlling the functionality of the process of the current memories as disclosed in Column 2, Lines 35-48**)

Yamaguchi and Hughes teach in Claim 3:

A current output type drive circuit as set forth in claim 2, wherein
said current sampling circuit includes a first current memory and a second current memory (**Figure 4 shows first and second current memories M41 and M42**), and

said control circuit outputs to said current sampling circuit said control signal so as to alternately perform a write operation of the reference current input from said reference current

input terminal and a read operation of the written reference current on said first current memory and second current memory. **(It is obvious to one of skill that there is a control means for controlling the functionality of the process of the current memories as disclosed in Column 2, Lines 35-48. As for the alternating manner between reading and writing, this section discloses that during a first phase, there is writing to a first current memory, during a second phase, there is writing to the second memory while reading from the first memory and this repeats. This shows an alternating manner between the reading and writing operation. The combination with Yamaguchi teaches of using the sampling and holding circuit, including these memories, within the reference current generation circuit 12)**

Yamaguchi and Hughes teaches in Claim 4:

A current output type drive circuit as set forth in claim 2, wherein said output means includes a plurality of current output type digital/analog conversion circuits and the circuit comprises means for increasing the reference current read from the current memory of the current sampling circuit of said reference current source circuit to a plurality of reference currents by further copying or distributing them by time division, and said plurality of reference currents are supplied to said plurality of digital/analog conversion circuits. **(D/A converters, such as shown in Figure 4 of Hughes, are well known in the art for converting the signal and Examiner asserts Official Notice to the common use of these. Please note that is used in conjunction with the current memories. As for time division, Figure 1 of Yamaguchi shows a reference current generation circuit 12 which is used to send various signals to each of the**

drivers. Furthermore, Hughes teaches of different phases in which data is sent to the current memories. Both these are examples of time division driving)

Yamaguchi teaches in Claim 7:

A current output type drive circuit for outputting a drive current to a driven object shared by being divided into a plurality of areas (**Figure 1 shows the current drivers used to drive the EL devices 51, 52, etc (read as a plurality of areas) ,**

comprising a plurality of drivers arranged corresponding to each the shared area of the driven object (**Figure 1, driver ICS 1, 2 and 3, Column 5, Lines 41-46)**,

each driver comprising

an output means for outputting a supplied reference current as a drive current to the corresponding shared area of the driven object (**Figure 1, output terminals 001-064, Column 5, Lines 41-46. The terminals output the current from the driver circuits to the pixel elements) and**

a reference current source circuit (**Figure 1, reference current generation circuit 12)**

the reference current input terminal being connected to a reference current input terminal of another driver by a common current interconnect (**Figure 1, the reference current generation circuit 12 branches and inputs to each of the drivers. The common interconnect is shown in Figure 1 which connects the reference current generation circuit 12 which sends multiple current lines to the current driver circuits)**; but

Yamaguchi does not explicitly teach the reference current source circuit is used “for sampling and holding the reference current input from a reference current input terminal, then supplying the same to the output means.”

However, sampling and holding circuitry and means is well known in the art, in conjunction with current mirrors, taught by Yamaguchi and disclosed in Figure 3, which shows circuitry within the reference current generation circuit 12. In addition, Yamaguchi teaches of the reference current input terminals IREF as shown in Figures 1 and 2.

To emphasize on this, in the same field of endeavor, current circuitry, Hughes teaches of using current memories M41 and M42 to sample and hold the input current sample, (Hughes, Column 2, Lines 35-48). During the four phases, the two memories sample and store (read as held) and then outputted accordingly. The reference terminals of Yamaguchi connect to the reference current generation circuit 12 and the sampling and holding means are processed within 12 and then output accordingly.

Therefore, it would be obvious to one of ordinary skill at the time of the invention to integrate the sampling and holding means by using the current memories, as taught by Hughes, with Yamaguchi's circuitry, with the motivation that is sampling and holding is a well known technique in the art. KSR teachings provide many principles here, such as known technique, simple substitution of parts, with regards to implementing the circuitry, suggestion in the prior art, Yamaguchi, etc. Applicant has also noted that this is well known as well. As for

implementing them with the current memories, Hughes notes that by using two memories, data will not be corrupted, so data loss can be prevented, (Hughes, Column 2, Lines 4-19)

Yamaguchi teaches in Claim 8:

A current output type drive circuit as set forth in claim 7, wherein each driver fetches said reference current from said reference current input terminal to said reference current source circuit when receiving a signal indicating start of distribution of the reference current and outputs the signal indicating the start of distribution of reference current to the driver circuit of the next stage. (**Figure 1, control circuit 11 for on-off controlling of the driving current in correspondence with an input signal, Column 5, Lines 39-50. These signals are well known for enabling the correct drivers and periods. This figure also shows the various terminals attached from the reference current generation circuit 12)**

Yamaguchi and Hughes teach in Claim 9:

A current output type drive circuit as set forth in claim 8, wherein each driver comprises a data memory, writes input data into said data memory when receiving a first signal indicating start of writing of data and outputs said first signal indicating start of writing of data to the driver of the next stage and fetches said reference current from said reference current input terminal to said reference current source circuit in synchronization with said first signal when receiving a second signal indicating start of distribution of reference current and outputs said second signal indicating start of distribution of reference current to the driver circuit of the next stage.

(Figures 1 and 2 of Yamaguchi show the drivers and the construction of the drivers. These

include a latch and register, serving as the data memory. The various signals shown in Figure 1 control the drivers and periods and the distribution of the reference current comes from the reference current generation circuit 12 which is sent to each driver through the terminals)

Yamaguchi and Hughes teach in Claim 10:

A current output type drive circuit as set forth in claim 7, wherein said reference current source circuit (**Yamaguchi, Figure 1, reference current generation circuit 12**) comprises at least:

a current sampling circuit including a current memory for sampling and holding said reference current in accordance with a control signal (**Hughes, Figure 4 shows current memory M41**) and

a control circuit for outputting to said current sampling circuit a control signal for controlling write and read operations of said reference current of the current memory of said current sampling circuit. (**Hughes, Figure 4 shows the switches for each memory. It is obvious to one of skill that there is a control means for controlling the functionality of the process of the current memories as disclosed in Column 2, Lines 35-48**)

Hughes teaches in Claim 11:

A current output type drive circuit as set forth in claim 10, wherein
said current sampling circuit includes a first current memory and a second current memory (**Figure 4 shows first and second current memories M41 and M42**), and

said control circuit outputs to said current sampling circuit said control signal so as to alternately perform a write operation of the reference current input from said reference current input terminal and a read operation of the written reference current on said first current memory and second current memory. **(It is obvious to one of skill that there is a control means for controlling the functionality of the process of the current memories as disclosed in Column 2, Lines 35-48. As for the alternating manner between reading and writing, this section discloses that during a first phase, there is writing to a first current memory, during a second phase, there is writing to the second memory while reading from the first memory and this repeats. This shows an alternating manner between the reading and writing operation. The combination with Yamaguchi teaches of using the sampling and holding circuit, including these memories, within the reference current generation circuit 12)**

Yamaguchi and Hughes teaches in Claim 12:

A current output type drive circuit as set forth in claim 10, wherein said output means includes a plurality of current output type digital/analog conversion circuits and the circuit comprises means for increasing the reference current read from the current memory of the current sampling circuit of said reference current source circuit to a plurality of reference currents by further copying or distributing them by time division, and said plurality of reference currents are supplied to said plurality of digital/analog conversion circuits. **(D/A converters, such as shown in Figure 4 of Hughes, are well known in the art for converting the signal and Examiner asserts Official Notice to the common use of these. Please note that is used in conjunction with the current memories. As for time division, Figure 1 of**

Yamaguchi shows a reference current generation circuit 12 which is used to send various signals to each of the drivers. Furthermore, Hughes teaches of different phases in which data is sent to the current memories. Both these are examples of time division driving)

Yamaguchi teaches in Claim 13:

A current output type drive circuit as set forth in claim 7, wherein at least the reference current source circuit of the driver serving as a master includes a reference current source circuit generating a reference current and supplying it to said common current interconnect. (**Figure 1 shows the reference current generation circuit 12 acting as a ‘master’ circuit by applying current to each of the drivers. The interconnect is shown branching to all the drivers)**

Yamaguchi teaches in Claim 14:

A current output type drive circuit as set forth in claim 10, wherein at least the reference current source circuit of the driver serving as a master includes a reference current source circuit generating a reference current and supplying it to said common current interconnect. (**Figure 1 shows the reference current generation circuit 12 acting as a ‘master’ circuit by applying current to each of the drivers. The interconnect is shown branching to all the drivers)**

Yamaguchi teaches in Claim 17:

A current output type drive circuit as set forth in claim 7, wherein the interconnect of said reference current is arranged between power supply interconnects for shield. (**Figure 1 shows the interconnect lines in between each driver and the power supply Vcc as shown in Figure**

3. Column 7, Lines 12-24. The structure of the interconnect is the same and the shielding, or insulating structure is well known in the art and Examiner takes Official Notice as to the use of insulating layers used to shield the drivers)

Yamaguchi teaches in Claim 18:

A current output type drive circuit as set forth in claim 7, wherein the interconnect of said reference current, when a multilayer interconnect including a power supply layer for shield, is arranged at a top layer of said power supply layer for shield. (**Figure 1 of Yamaguchi shows the interconnect and the use of insulating layers is well known in the art and Examiner has asserted Official Notice to this above)**

Yamaguchi teaches in Claim 19:

A current output type drive circuit as set forth in claim 7, further comprising means for suppressing great fluctuations of the potential of said common reference current interconnect when the circuits sampling and holding the reference currents of the drivers are all off. (**Figure 1 shows the control circuits for on-off controlling of the driving current in correspondence with an input signal, Column 5, Lines 39-50. When off, there would obviously be a suppression of potential. Furthermore, the signals as shown in Figure 1 are responsible for the application of voltages and currents)**

Yamaguchi teaches in Claim 20:

A current output type drive circuit as set forth in claim 12, wherein

said means increasing said reference current to a plurality of reference currents comprises a current mirror circuit configured by a constant current source (**Column 6, Lines 57-63, current mirror circuit 120 from a constant current driver circuit 10**) including resistor elements arranged at the input stage and a plurality of reference current sources including resistor elements arranged at the output stage in parallel so as to correspond to the output parts of said output means (**Figure 1 shows the plurality of sources arranged in parallel to the output terminals. Column 5, Lines 57-65 disclose of a reference resistance which is mounted on the drivers and includes the current drivers**), and

the resistor elements of the reference current sources arranged at the two ends among said plurality of reference current sources are arranged close to the resistor elements of said constant current source. (**Column 5, Lines 57-65 disclose resistances 13 which is wired to each of the drivers, thus affecting them**)

Yamaguchi teaches in Claim 21:

A current output type drive circuit as set forth in claim 20, wherein the resistor elements forming the reference current sources are laid out divided and cross-laced. (**Figure 1, Column 5, Lines 57-65 shows the resistance 13 to be 'divided' and wired to each of the drivers for the intended effect**)

Yamaguchi teaches in Claim 22:

A display device for outputting a drive current to a shared area of a display panel shared by being divided into a plurality of areas (**Figure 1 shows the current drivers used to drive the EL devices 51, 52, etc (read as a plurality of areas) ,**

comprising a plurality of drivers arranged corresponding to each the shared area of the display panel (**Figure 1, driver ICS 1, 2 and 3, Column 5, Lines 41-46),**

each driver comprising an output means for outputting a supplied reference current to a corresponding shared area of the driven object (**Figure 1, output terminals 001-064, Column 5, Lines 41-46. The terminals output the current from the driver circuits to the pixel elements) and**

a reference current source circuit (**Figure 1, reference current generation circuit 12. It is connected to each of the drivers); but**

Yamaguchi does not explicitly teach the reference current source circuit is used “for sampling and holding the reference current input from a reference current input terminal, then supplying the same to the output means.”

However, sampling and holding circuitry and means is well known in the art, in conjunction with current mirrors, taught by Yamaguchi and disclosed in Figure 3, which shows circuitry within the reference current generation circuit 12. In addition, Yamaguchi teaches of the reference current input terminals IREF as shown in Figures 1 and 2.

To emphasize on this, in the same field of endeavor, current circuitry, Hughes teaches of using current memories M41 and M42 to sample and hold the input current sample, (Hughes, Column 2, Lines 35-48). During the four phases, the two memories sample and store (read as held) and then outputted accordingly. The reference terminals of Yamaguchi connect to the reference current generation circuit 12 and the sampling and holding means are processed within 12 and then output accordingly.

Therefore, it would be obvious to one of ordinary skill at the time of the invention to integrate the sampling and holding means by using the current memories, as taught by Hughes, with Yamaguchi's circuitry, with the motivation that is sampling and holding is a well known technique in the art. KSR teachings provide many principles here, such as known technique, simple substitution of parts, with regards to implementing the circuitry, suggestion in the prior art, Yamaguchi, etc. Applicant has also noted that this is well known as well. As for implementing them with the current memories, Hughes notes that by using two memories, data will not be corrupted, so data loss can be prevented, (Hughes, Column 2, Lines 4-19)

Yamaguchi teaches in Claim 23:

A display device for outputting a drive current to a shared area of a display panel shared by being divided into a plurality of areas (**Figure 1 shows the current drivers used to drive the EL devices 51, 52, etc (read as a plurality of areas)),**

comprising a plurality of drivers arranged corresponding to each the shared area of the display panel (**Figure 1, driver ICS 1, 2 and 3, Column 5, Lines 41-46),**

each driver comprising

an output means for outputting a supplied reference current to a corresponding shared area of the driven object (**Figure 1, output terminals 001-064, Column 5, Lines 41-46. The terminals output the current from the driver circuits to the pixel elements**) and

a reference current source circuit (**Figure 1, reference current generation circuit 12**)

the reference current input terminal being connected to a reference current input terminal of another driver by a common current interconnect (**Figure 1, the reference current generation circuit 12 branches and inputs to each of the drivers**); but

Yamaguchi does not explicitly teach the reference current source circuit is used “for sampling and holding the reference current input from a reference current input terminal, then supplying the same to the output means.”

However, sampling and holding circuitry and means is well known in the art, in conjunction with current mirrors, taught by Yamaguchi and disclosed in Figure 3, which shows circuitry within the reference current generation circuit 12. In addition, Yamaguchi teaches of the reference current input terminals IREF as shown in Figures 1 and 2.

To emphasize on this, in the same field of endeavor, current circuitry, Hughes teaches of using current memories M41 and M42 to sample and hold the input current sample, (Hughes, Column 2, Lines 35-48). During the four phases, the two memories sample and store (read as held) and then outputted accordingly. The reference terminals of Yamaguchi connect to the reference

current generation circuit 12 and the sampling and holding means are processed within 12 and then output accordingly.

Therefore, it would be obvious to one of ordinary skill at the time of the invention to integrate the sampling and holding means by using the current memories, as taught by Hughes, with Yamaguchi's circuitry, with the motivation that is sampling and holding is a well known technique in the art. KSR teachings provide many principles here, such as known technique, simple substitution of parts, with regards to implementing the circuitry, suggestion in the prior art, Yamaguchi, etc. Applicant has also noted that this is well known as well. As for implementing them with the current memories, Hughes notes that by using two memories, data will not be corrupted, so data loss can be prevented, (Hughes, Column 2, Lines 4-19)

Yamaguchi teaches in Claim 24:

A display device as set forth in claim 23, wherein each driver fetches said reference current from said reference current input terminal to said reference current source circuit when receiving a signal indicating start of distribution of reference current and outputs the signal indicating start of distribution of reference current to the driver circuit of the next stage. (**Figure 1, control circuit 11 for on-off controlling of the driving current in correspondence with an input signal, Column 5, Lines 39-50. These signals are well known for enabling the correct drivers and periods. This figure also shows the various terminals attached from the reference current generation circuit 12)**

Yamaguchi and Koyama teach in Claim 25:

A display device as set forth in claim 23, wherein each driver comprises a data memory, writes input data into said data memory when receiving a first signal indicating start of writing of data and outputs said first signal indicating start of writing of data to the driver of the next stage and fetches said reference current from said reference current input terminal to said reference current source circuit in synchronization with said first signal when receiving a second signal indicating start of distribution of reference current and outputs said second signal indicating start of distribution of reference current to the driver circuit of the next stage. **(Figures 1 and 2 of Yamaguchi show the drivers and the construction of the drivers. These include a latch and register, serving as the data memory. The various signals shown in Figure 1 control the drivers and periods and the distribution of the reference current comes from the reference current generation circuit 12 which is sent to each driver through the terminals)**

Yamaguchi teaches in Claim 26:

A display device as set forth in claim 23, wherein the interconnect of said reference current is arranged between power supply interconnects for shield. **(Figure 1 shows the interconnect lines in between each driver and the power supply Vcc as shown in Figure 3. Column 7, Lines 12-24. The structure of the interconnect is the same and the shielding, or insulating structure is well known in the art and Examiner takes Official Notice as to the use of insulating layers used to shield the drivers)**

Yamaguchi teaches in Claim 27:

A display device as set forth in claim 23, wherein the interconnect of said reference current, when a multilayer interconnect including a power supply layer for shield, is arranged at a top layer of said power supply layer for shield. **(Figure 1 of Yamaguchi shows the interconnect and the use of insulating layers is well known in the art. Examiner has asserted Official Notice to this as noted above)**

Yamaguchi teaches in Claim 28:

A display device as set forth in claim 23, further comprising means for suppressing great fluctuations of the potential of said common reference current interconnect when the circuits sampling and holding the reference currents of the drivers are all off. **(Figure 1 shows the control circuits for on-off controlling of the driving current in correspondence with an input signal, Column 5, Lines 39-50. When off, there would obviously be a suppression of potential. Furthermore, the signals as shown in Figure 1 are responsible for the application of voltages and currents)**

Response to Arguments

6. Applicant's arguments have been considered persuasive, so the finality of the last rejection has been removed and this non-final action will be sent. With regards to Claim 1, a new secondary reference has been combined with Yamaguchi, so Applicant's arguments with respect to Koyama are considered moot. This is also the case with some of Applicant's other arguments.

Conclusions

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dennis P. Joseph whose telephone number is 571-270-1459. The examiner can normally be reached on Monday-Friday, 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on 571-272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DJ

/Amr Awad/

Supervisory Patent Examiner, Art Unit 2629

